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| EXAMINER | |
|---|---|
| MOON, SEOKYUN | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/621,250 | LEE ET AL. | |
| | Examiner | Art Unit | |
| | Seokyun Moon | 2629 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 June 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3,5 and 13-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-20* is/are allowed.

6)☒ Claim(s) *1,3,5,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

**DETAILED ACTION**

***Response to Arguments***

1. The Applicant's arguments filed June 30, 2009 have been fully considered.

In the Applicant's arguments, the Applicant explains the teaching of the prior arts disclosed in the Background section of the specification of the instant application [Remarks: pg 6 - pg 7 1st partial paragraph] and asserts that the prior art cited by the Examiner (US 2003/0117356, herein after, "*Moon*") cannot teach one of the limitations of claim 1 since the operation principle of the device of Moon is similar to the teaching of the prior art disclosed in the instant application [Remarks: pg 7 1st full paragraph - the last paragraph]. Specifically, the Applicant points out, "*As Moon specifically teaches using "compensating resistor" to teach TCP 46A-46D to address this problem of voltage drop in the signal line pattern due to its inherent resistance, Moon's TCP 46A-46D does not require or include the following sequence recognition limitation in each of TCPs 46A-46D recited in claim 1 as follows: - a sequence recognition unit for recognizing sequence of a pertinent gate driver IC from a plurality of gate driver ICs by a pulse width of a vertical start signal inputted in synchronization with a vertical synchronous signal, and generating a carry signal and location data of the pertinent gate driver IC -*" [Remarks: pg 8 2nd full paragraph].

Examiner respectfully disagrees.

Prior to the discussion of the Applicant's arguments regarding the Moon reference, Examiner respectfully submits that only the claim limitation, "*a sequence*

*recognizing unit for recognizing sequence of a pertinent gate driver IC from a plurality of gate driver ICs*" will be discussed with respect to the Applicant's arguments regarding the Moon reference since the previous Office action does not indicate that Moon teaches all of the claim limitation argued by the Applicant, but teaches only the above claim limitation. Furthermore, Examiner respectfully submits that regardless of whether the teaching of the prior art acknowledged by the Applicant is similar to the teaching of Moon or not, the above limitation of claim 1 does not differentiate the instant invention from the prior art acknowledged by the Applicant and Moon. An explanation regarding how Moon teaches the above claim limitation is provided below.

Moon teaches a plurality of gate driver ICs being arranged sequentially in a liquid crystal display driving apparatus, as shown on figure 3. Moon also teaches gate control signals such as gate start pulse, gate shift clock, and gate enable signals generated by a timing controller being transmitted through gate low voltage transmission lines "*VGLL1*" to "*VGLL4*" [par. (0054) lines 1-9 and fig. 3]. Thus, the plurality of gate driver ICs of Moon output gate signals sequentially in response to receiving gate start pulse, gate shift clock, and gate enable signals. In other words, gate start pulse, gate shift clock, and gate enable signals are the signals for activating the function of the gate driver ICs, i.e. outputting gate signals, based on the sequence of each of the gate driver ICs. Thus, the means for receiving the gate start pulse, gate shift clock, and gate enable signals and triggering the output of gate signals in response to receiving the gate start pulse, gate shift clock, and gate enable signals are the means for recognizing the sequence of each of the gate driver ICs from a plurality of gate driver ICs. In a

summary, each of the plurality of gate driver ICs outputs gate signals at certain timings different from the timings of outputting gate signals by other gate driver ICs and the gate start pulse, gate shift clock, and gate enable signals are the signals indicating the timing of activating each of the plurality of gate driver ICs and the timing of activating each of the plurality of gate driver ICs is equivalent to the sequence of each of the plurality of gate driver ICs, and thus the means for receiving the gate start pulse, gate shift clock, and gate enable signals and triggering the output of gate signals in response to receiving the gate start pulse, gate shift clock, and gate enable signals are the means for recognizing the sequence of each of the gate driver ICs from a plurality of gate driver ICs.

The Applicant further argues, "*The mere fact that Nishtani teaches a counter that, however, is applied in a totally different design for a totally different purpose than the presently claimed invention does not provide sufficient rationale that the counter of Nishtani can be modified or combined with Moon...*" [Remarks: pg 9 3rd full paragraph].

However, Examiner respectfully submits that the Applicant's above assertion is incorrect. The fact of whether the counter of Nishitani is applied in a totally different design for a totally different purpose than the presently claimed invention or not does not determine whether the counter of Nishitani can be combined with Moon. In other words, the difference between the cited prior art and the instant invention does not determine whether the cited prior art is combinable with another cited prior art or not. Moon teaches a means for controlling the timing of the operation of one of a plurality of gate drivers, but does not teach the specific structure of the means and how the means

is operated. Nishitani teaches the concept of including a counter in one of a plurality of scanning drivers as a means for controlling the timing of the operation of the scanning driver. Since both of the means of Moon and Nishitani are configured to perform same function, it would have been obvious to one of ordinary skilled in the art at the time of the invention to use the specific structure and the operation means of Nishitani as the structure and the operation method of the means for controlling the operation of the gate driver taught by Moon.

For the foregoing reasons, Examiner respectfully submits that the Applicant's arguments are not persuasive.

***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1**, **3**, **5**, and **21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Moon (US 2003/0117356) in view of Nishitani (US 5,764,212).

As to **claim 1**, Moon teaches a liquid crystal display driving device [fig. 3 and par. (0043)] generating gate-on/off signals to drive liquid crystal comprising [par. (0007) lines 8-10, note that even though the teachings in the cited paragraph are mentioned under "*Description of the Related Art*" section, Moon's liquid crystal display driving device is also operated based on the teachings]:

a sequence recognition unit (means included in one of "*gate TCPs 46A-46D*", receiving one of "*gate start pulse*" and "*gate enable signal*") [fig. 3 and par. (0054) lines 1-9] for recognizing sequence of a pertinent gate driver IC from a plurality of gate driver ICs (Note that "*gate start pulse*" and "*gate enable signal*" correspond to a location of a gate driver IC within a plurality of gate driver ICs); and

a gate-off voltage generation unit (a combination of means for generating gate driving signals within one of "*gate driver ICs 48A-48D*" and a compensating resistor corresponding to the one of "*gate driver ICs 48A-48D*") [fig. 3 and par. (0055)] for receiving a first gate-off voltage ("*gate low voltage*", i.e. "*Vg1*")) [par. (0057)] and location data (one of "*gate start pulse*" and "*gate enable signal*") of the pertinent gate driver IC, and outputting a second gate-off voltage which is generated by subtracting a voltage attenuation quantity corresponding to the location data of the gate driver IC from the first gate-off voltage [par. (0057) lines 6-10].

Moon does not expressly teach the sequence recognition unit recognizing sequence of a pertinent gate driver IC from a plurality of gate driver ICs by a pulse width of a vertical start signal inputted in synchronization with a vertical synchronous signal and generating a carry signal and location data of the pertinent gate driver IC.

However, Nishitani teaches a concept of including a sequence recognition unit (a combination of "*counter 92*" and "*decoder 93*") [fig. 25] in a gate driver ("*gate driver 89-1*") [figs. 24 and 25], which recognizes sequence of the gate driver among a plurality of gate drivers by a pulse width of a vertical start signal ("*enable input signal 91*") [fig. 25] and generating a carry signal ("*enable output signal 97*") and location data (the signal

outputted from the "*decoder 93*") of the gate driver [col. 21 lines 24-37], wherein the sequence recognition unit [Nishitani: fig. 25] comprising:

a m-bit counter (Nishitani: "*counter 92*") [Nishitani: fig. 25] for estimating the pulse width of the vertical start signal (Nishitani: "*enable input signal 91*") [Nishitani: col. 21 lines 24-37, note that, in the device of Moon as modified by Nishitani, the m-bit counter is activated based on whether the enable input signal is high or not] inputted in synchronization with the vertical synchronous signal (as discussed with respect to the rejection of claim 1), and generating the location data of the pertinent gate driver IC; and

a carry signal generation unit (Nishitani: the means included in the "*counter 92*" generating "*enable output signal 97*") [Nishitani: fig. 25] for generating the carry signal (Nishitani: "*enable output signal 97*") that a vertical start signal (Nishitani: "*enable output signal 97*") thereof has a pulse width changed on the basis of location of the pertinent gate driver IC [Nishitani: col. 21 lines 24-37, note that, in Nishitani's driving device, the pulse width becomes zero when the gate driver IC is not selected].

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement Nishitani's sequence recognition means into Moon's gate driver ICs (i.e. implementing the structure of Nishitani's sequence recognition means shown on fig. 25 into Moon's gate driver ICs), which recognizes sequence of a gate driver IC among a plurality of gate driver ICs by a pulse width of a vertical start signal and generates a carry signal and location data, in order to allow Moon's liquid crystal display driving device to control and process the gate on/off voltages outputted from the plurality of gate driver ICs precisely.

Moon as modified by Nishitani inherently teaches the vertical start signal being inputted in synchronization with a vertical synchronous signal because the driving device would not output image data to column/data electrodes at correct timings if the signal activating the gate driver ICs, i.e. the vertical start signal, is not synchronized to the vertical synchronous signal.

As to **claim 3**, Moon as modified by Nishitani teaches that the carry signal (Nishitani: "*enable input signal 97*") [Nishitani: fig. 25] is provided to the next gate driver IC so as to be used as a vertical start signal [Nishitani: col. 21 lines 24-37].

As to **claim 5**, Moon as modified by Nishitani teaches that the at least one state signal is determined according to resolution, size of a liquid crystal panel, and characteristic of a signal line pattern (Note that all of gate signal, gate start pulse, and gate enable signal are determined based on the resolution, size of a liquid crystal panel, and characteristics of a signal line pattern because if the resolution or the size of a liquid crystal panel or the number of signal line is increased, then the timing of applying the gate signal and the gate start pulse and the gate enable signal must be changed in order to apply image data to pixels of the display at correct timings.).

As to **claim 21**, Moon as modified by Nishitani teaches the gate-off voltage generation unit receives at least one state signal (Moon: any one of gate signal, gate start pulse, and gate enable signal) [Moon: par. (0054)] (Note that since any one of gate signal, gate start pulse, and gate enable signal controls/changes a state of a component within the display, it would be reasonable to construe any one of the signals as a state signal).

4. **Claims 21** and **22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Moon and Nishitani as applied to claims 1-3 above, and further in view of Sakamoto (US 6,049,319).

As to **claim 21**, Moon as modified by Nishitani does not expressly teach the gate-off voltage generation unit receiving at least one state signal.

However, Sakamoto teaches the concept of having a gate-off voltage generation unit (a combination of "*20*", "*22*", and "*3*") [fig. 5] receiving a state signal (the signal inputted to "*20*") and adding a compensation value corresponding to the state signal to a gate-off voltage, thereby generating a second gate-off voltage [col. 5 lines 51-62].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the gate-off voltage generation unit of Moon as modified by Nishitani to receive a state signal and to add a compensation value corresponding to the state signal to the gate-off voltage, thereby to generate a second gate-off voltage, as taught by Sakamoto, in order to reduce cross talk occurred in the display and thus to improve the quality of images to be displayed.

As to **claim 22**, Moon as modified by Nishitani and Sakamoto teaches that the gate-off voltage generation unit subtracts voltage attenuation quantity corresponding to location data of the gate driver IC from an inputted gate-off voltage [Moon: par. (0057) lines 6-10, as discussed with respect to the rejection of claim 1] and adds a compensation value corresponding to one of the at least one state signal to the subtracted gate-off voltage, thereby generating the second gate-off voltage [Sakamoto: col. 5 lines 51-62, as discussed with respect to the rejection of claim 21].

***Allowable Subject Matter***

5. **Claims 13-20** are allowed.

***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seokyun Moon whose telephone number is 571-272-5552. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 572-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

November 02, 2009
/S. M./
Examiner, Art Unit 2629

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629